Wafer Charging in Process Equipment and its Relationship to GMR Heads Charging Damage

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Abstract – Significant amount of know-how and understanding of device charging damage in processing equipment exists in CMOS IC manufacturing. This paper introduces the basic charging mechanisms responsible for gate oxide damage in CMOS ICs, illustrates these mechanisms with examples of measurements obtained in contemporary IC processing equipment, describes a wafer charging characterization method successfully used by integrated circuit and equipment manufacturers to quantify wafer charging in process equipment, and shows how this knowledge could be applied to the control of charging damage in GMR heads wafer processing.

Introduction

To achieve increasing storage densities in magnetic disk drives, it has become necessary to employ GMR read heads whose construction requires extremely thin insulating layers and extremely small feature sizes. Since the process tools used in the manufacture of GMR heads are ion beam and plasma-based, possible wafer charging in these tools can damage the insulators during wafer manufacturing, reducing GMR head manufacturing yields and/or impacting GMR head reliability.

Although process-induced charging damage is a relatively recent issue in read head manufacturing, charging damage to thin insulators has been a vexing problem in ion beam and plasma-based process tools used in CMOS integrated circuit manufacturing for almost two decades. Moreover, although IC's and read heads are vastly different products, similar structural features are fabricated during wafer manufacturing of both CMOS ICs and GMR heads. Consequently, the process charging-induced damage mechanisms should be similar, and a significant amount of understanding and know-how related to the measurement and control of wafer charging in CMOS IC process equipment should be applicable to the measurement and control of wafer charging in GMR head manufacturing.

Given this situation, the purpose of this paper is (a) to introduce the basic charging mechanisms responsible for gate oxide damage in CMOS ICs, (b) to illustrate these mechanisms with measurements obtained in contemporary IC processing equipment, (c) to describe a wafer charging characterization method successfully used by integrated circuit and equipment manufacturers to quantify wafer charging in process equipment, and (d) to relate the results and know-how accumulated in CMOS IC manufacturing to the control of wafer charging damage in GMR head manufacturing.

I. Basics of Charging Damage

Although the understanding of damage to insulators during wafer processing can be complicated by many details, the underlying concepts are relatively simple. Damage to thin insulators sandwiched between a conductive substrate and isolated conductive electrodes on the surface of a wafer occurs due to ***current flow*** through the insulator, driven by a potential difference between the surface electrode and the substrate [1]. Even when the substrate is electrically floating, differences in potential between electrodes located in different portions of a wafer can cause current flow from one set of electrodes to the other via the insulator and the substrate.

During wafer processing, these global (wafer scale) potential differences are caused by global non-uniformities in plasma density and/or electron temperature [2] or, in the case of ion-beam equipment, by spatially imperfect neutralization of the ion beam. Both of these mechanisms cause imbalances in ion and electron fluxes that give rise to different electrode-substrate potentials over large areas of the wafer. Charging damage in processes where the entire electrodes are exposed, such as resist stripping [3] and

insulator depositions [4], is typically associated with global variations in surface charging.

However, even in uniform plasmas, highly localized charging due to local imbalance of ion and electron fluxes associated with holes-in-insulator topographical features may cause local insulator damage. This localized charging (called "electron shading") [5] is due to negative charging of the insulator (e. g. resist) which prevents low energy electrons from reaching the bottom of the hole to neutralize the positive ion flux, thereby causing net positive charging at the bottom of the hole. The magnitude of this fundamental effect increases with increasing aspect (height/width) ratio. Charging damage in etching processes is caused by a combination of global and localized charging. The localized charging caused by "electron shading" is superimposed on the global charging effects.

II. Some Experimental Results

The charging behavior of ion milling tools used in the manufacture of GMR heads resembles wafer charging in high-current ion implanters used in the IC industry. When devices are under the beam in a high-current ion implanter, they experience positive charging due to the ion beam and the secondary electrons emitted from the surface of the wafer. When devices are outside the beam, they experience negative charging due to the "electron shower", or the plasma flood system, used to neutralize positive charging.

The balance between positive and negative charging, controlled by the "electron shower" or a plasma flood system, is illustrated in Figures 1a and 1b.

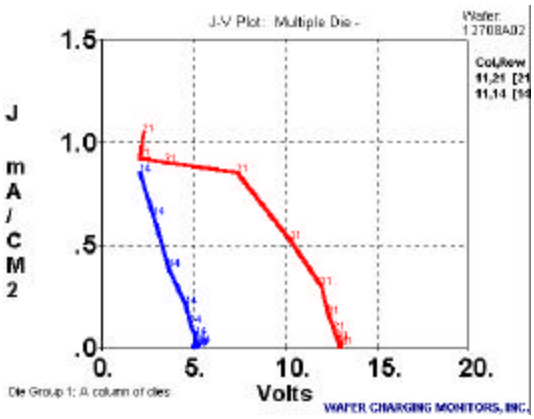

Figure 1a. Positive J-V plots recorded at two different locations on a wafer during a high current ion implant.

Higher positive charging in die (11,21), curve 21, shown in **Figure 1a**, is associated with lower negative charging, shown in **Figure 1b**. Conversely lower positive charging in die (11,14), curve 14, is associated with higher negative charging. In this case, the spatially non-uniform output of the electron shower thus gave rise to spatially non-uniform positive charging.

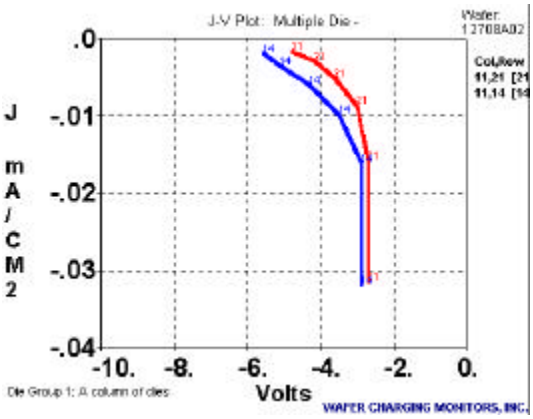

Figure 1b. Negative J-V plots recorded on the same wafer during a high current ion implant.

An example of charging damage to 70 A gate oxide in a plasma resist asher due to globally non-uniform charging is shown next. This example also illustrates that regions of highest surface-to-substrate potentials *are not necessarily* the regions of greatest charging damage. (High potentials alone are not sufficient to cause damage.)

Although the damage to the 70 A gate oxide capacitors occurred in the center of the wafer **[3]**, the highest potentials measured with a CHARM®-2 wafer occurred around the periphery of the wafer, as shown in **Figure 2a.** The negative potentials in the center of the wafer, shown in **Figure 2b,** were significantly lower.

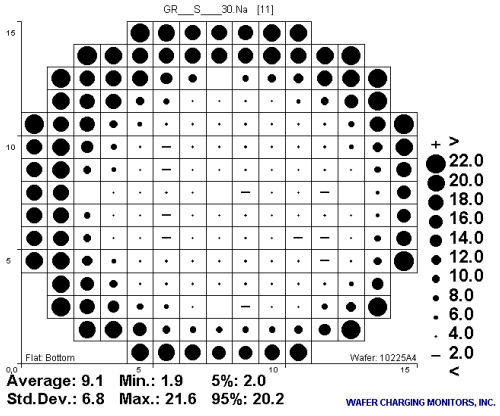

Figure 2a. Positive potentials recorded in a resist asher.

To understand why damage occurred in the center of the wafer, it is necessary to compare the positive and negative J-V characteristics of this charging source, shown in **Figure 2c.**

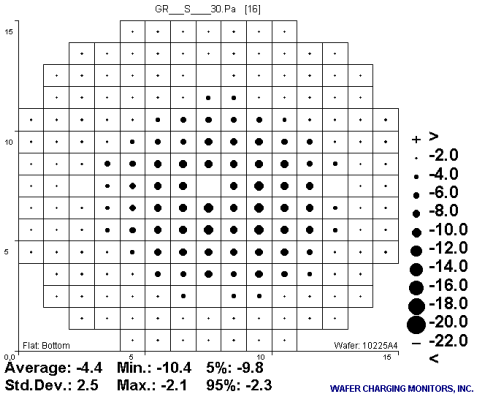

Figure 2b. Negative potentials recorded in a resist asher.

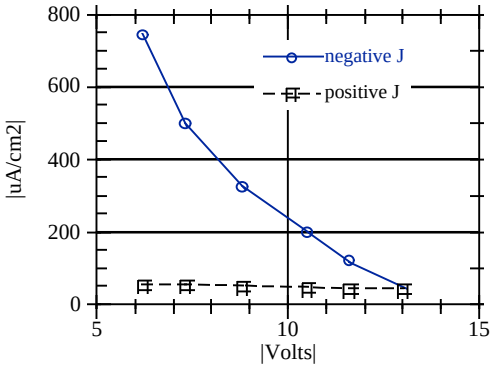

Figure 2c. Positive and negative current densities recorded in a resist asher. Positive J-V came from die around the periphery of the wafer. Negative J-V came from die in the center of the wafer.

This figure shows that the negative current density, recorded in the center of the wafer, was significantly higher than the positive current density, recorded around the periphery of the wafer. As should be expected, the damage to the 70 A gate oxide (which conducts significant current density below 10 V) occurred in the region of the highest ***current*** density**,** *not* in the region of the highest surface-to-substrate potential.

The localized charging effect ("electron shading") caused by hole-in-insulator topographies is illustrated in **Figures 3a, 3b, and 3c**. **Figure 3a** is a wafer map of positive potentials obtained in a plasma oxide etcher using a bare CHARM®-2 wafer (no topography). The potentials are low and uniform over the entire wafer, indicating good plasma uniformity.

On the other hand, **Figure 3b** is a wafer map of positive potentials obtained in the same oxide etcher using a CHARM®-2 wafer covered with photoresist with holes patterned in it using electron-beam lithography. Significantly elevated potentials in the different sites illustrate the effect of the twelve different designs which used different size and number of holes in resist over the charge-collection-electrodes.

Figure 3c illustrates the aspect-ratio dependence of the localized, topography-induced charging. Both peak potentials and current densities measured with the 0.3um hole pattern are higher than those obtained for the 0.6um hole pattern **[6]**.

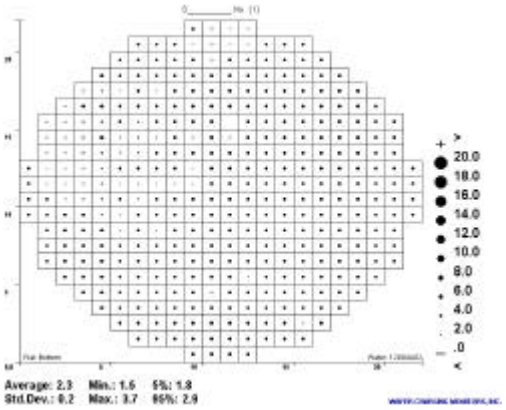

Figure 3a. Positive potentials in an oxide etcher obtained using a bare CHARM®-2 wafer.

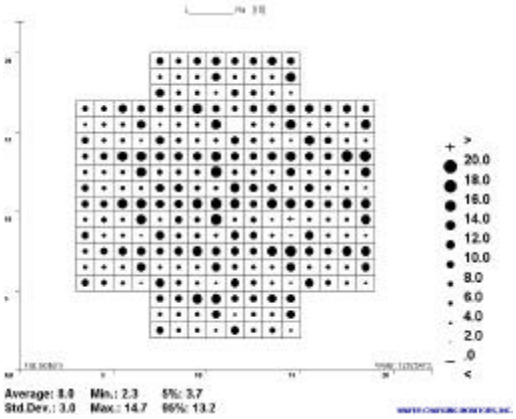

Figure 3b. Positive potentials in an oxide etcher obtained using a CHARM®-2 wafer covered with patterned resist.

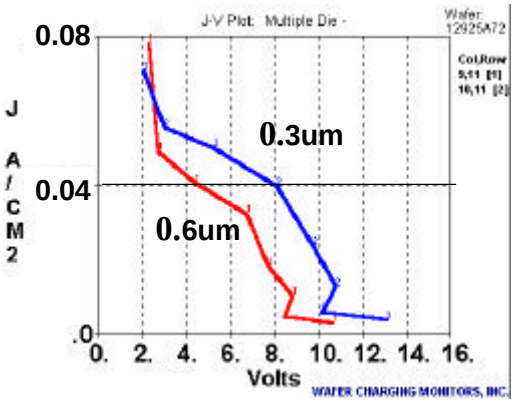

Figure 3c. Positive current densities vs. surface-substrate potential in 0.6 um holes and 0.3 um holes measured in an oxide etcher with a CHARM®-2 wafer covered with patterned resist.

Although the previous examples support the plasma non-uniformity and the "electron shading" damage models, additional effects occur for which adequate models have not been established. **Figures 4a-4d** compare positive potentials and J-V plots obtained in an oxide etcher with a bare CHARM®-2 wafer and a CHARM®-2 wafer covered with photoresist patterned with a product via mask **[7]**. The plasma non-uniformity, evident in the positive potentials and J-V plots obtained with a bare CHARM®-2 wafer, and shown in **Figures 4a and 4b,** are significantly amplified by the presence of the patterned photoresist, as shown in **Figures 4c and 4d.**

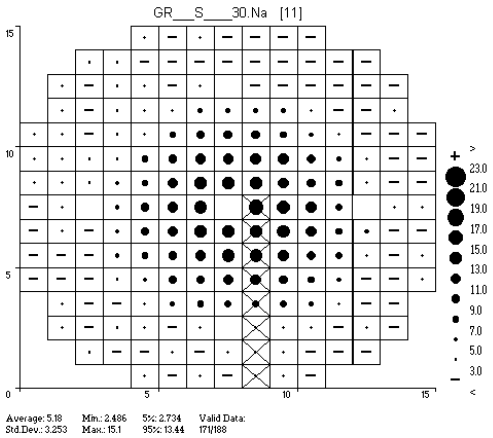

Figure 4a. Positive potentials on bare CHARM®-2 wafer; "X" indicates die locations selected for J-V plots in **Figure 4b.**

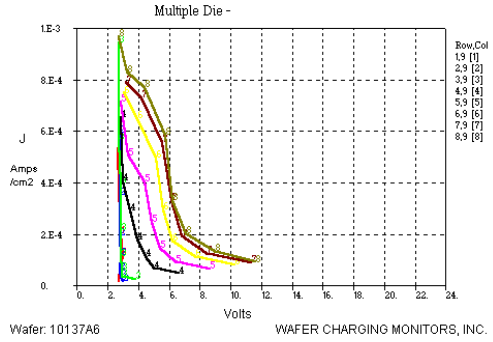

Figure 4b. Positive J-V plots obtained on bare CHARM®-2 wafer.

In particular, the positive J-V plots shown in **Figure 4d** were obtained from sensor locations coinciding with the product die 100um-wide scribe lanes. The dramatic increase in positive potentials and current densities in these locations cannot be attributed to the topography-dependent "electron shading" effect (the aspect ratio is very low). A quantitative model for this phenomenon has not been presented yet.

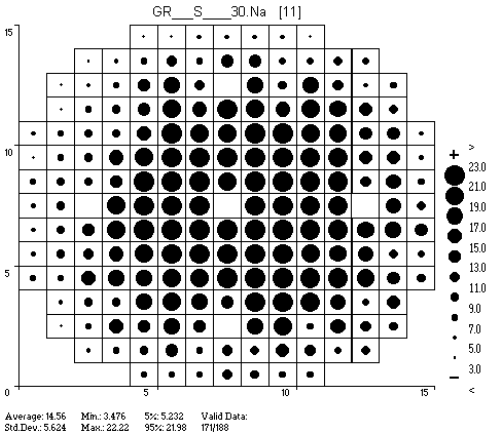

Figure 4c. Elevated positive potentials on CHARM®-2 wafer covered with resist patterned with product via mask.

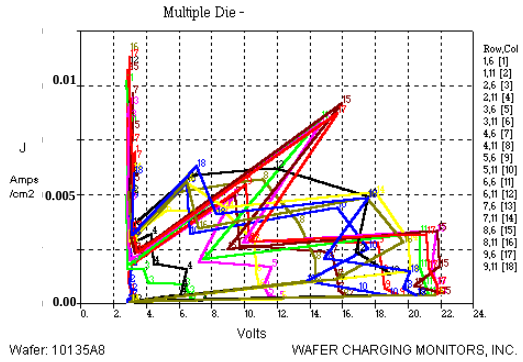

Figure 4d. Positive J-V plots obtained on wafer covered with resist patterned with product via mask. J-V plots are irregular due to mis-alignment of via mask and CHARM®-2 wafer layout.

III. Measurement Tools

As the resist asher example in **Figures 2a-2c** illustrates, charging ***currents*** are responsible for charging damage. Consequently, to adequately assess the charging damage tendency of a given process tool, it is essential to measure both potentials *and charging current densities* with sufficiently high spatial resolution using microscopic-size electrodes. Moreover, the entire probe should resemble a product wafer, since the on-wafer charging effects arise from the interaction of the wafer (and the devices on it) with the charging environment.

The most convenient, and the most widely used, probes of this kind are the CHARM®-2 monitors[1], which are implemented as monolithic silicon wafers populated with microscopic, EEPROM-based potential, charge-flux, and UV sensors **[8]**.

[1] CHARM®-2 monitors are available from Wafer Charging Monitors, Inc., Woodside, CA. CHARM® is a registered trademark of Wafer Charging Monitors, Inc.

CHARM®-2 potential sensors are implemented by connecting a charge collection electrode (CCE) on the surface of the wafer to the control-gate of an EEPROM transistor, as shown in **Figure 5a**.

In order to maximize the low-voltage sensitivity of the potential sensors, and to determine the polarity of the collected charge, the EEPROM transistors are programmed before use to either saturated positive or saturated negative threshold voltage states. Sensors whose EEPROM transistors are programmed to a saturated *positive* threshold state respond to *negative* potentials, while sensors whose EEPROM transistors are programmed to a saturated *negative* threshold state respond to *positive* potentials. The potential sensors are calibrated to measure the surface-substrate potential in volts [**8**].

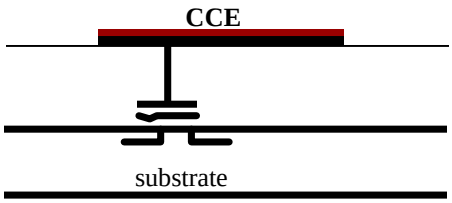

Figure 5a. CHARM®-2 potential sensor.

CHARM®-2 charge-flux sensors are implemented by adding current-sensing resistors between the CCE and the substrate of the potential sensors, as shown **Figure 5b**. In this configuration, EEPROM transistors measure the voltage across the current-sensing resistors, from which the current density is calculated. The charge-flux sensors are also implemented in pairs, where one set of sensors measures net negative charge flux and the second set of sensors measures net positive charge flux.

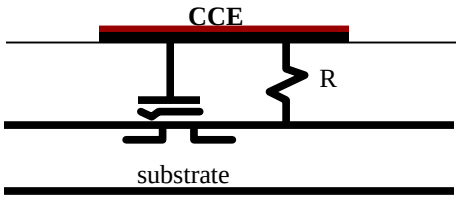

Figure 5b. CHARM®-2 charge-flux sensor.

The closely ratioed current-sensing resistors permit reconstruction of the J-V characteristics of the charging source as shown in **Figure 5c**. In the J-V plane, each resistor is represented by a straight line with a slope of 1/AR, where A is the area of the charge collecting electrode. Since the response of each sensor must lie on that line, each sensor provides one point in the J-V plane, and the collection of (J,V) values obtained from the set of CHARM®-2 current sensors allows re-construction of the positive or negative J-V characteristics of the charging source. The charge-flux sensors are calibrated to measure charge-flux in A/cm^2 [**8**].

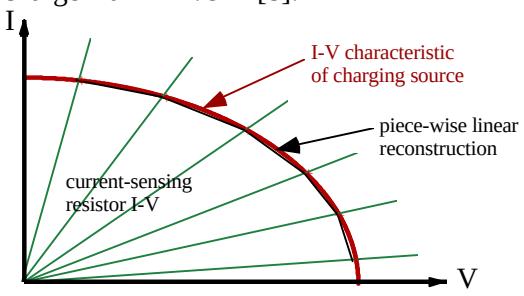

Figure 5c. Charge-flux sensors with different value current sensing resistors allow re-construction of the J-V characteristics of the charging source.

IV. Application to GMR Heads

The basics of wafer charging and process tool characterization described in this paper should be applicable to GMR head manufacturing due to the similarities it has with IC manufacturing. Certainly, many of the fabrication tools used in the GMR head industry are based on the same or similar physical principles as those used in the IC industry, so they should exhibit similar charging behavior. Consequently, the tool characterization methods described here should be applicable to GMR processing equipment.

The characterization parameters are also appropriate to GMR heads, since GMR dielectric damage is initiated by surface-to-substrate potentials [**9**] and is likely driven by charging currents. In addition, there exists the possibility of joule-heating damage to thin temperature-sensitive conductors, caused by charging currents. Therefore, in GMR head processes both wafer surface-to-substrate potentials and charge-fluxes need to be monitored.

Also, both technologies employ similar device structures which, from an electrostatics point of view, are capacitors using very thin dielectric layers whose integrity is critical to proper device operation. However, due to the difference in substrate material, the response of GMR heads to electrostatic effects, particularly charging transients, is simpler than the response of MOS transistors. Unlike the semiconductor substrate used in IC's, the GMR head's metallic substrate does not permit the formation of rectifying junctions and depletion/inversion layers that can modulate the voltage across the dielectric layers and make it difficult to predict the magnitude of stress applied to them. Consequently, the application of tool characterization results, such as those shown in this

paper, to prediction of GMR head damage should be both more direct and less prone to error.

However, we should also recognize some important differences which may require some modification in the interpretation of CHARM®-2 characterization results. Since it is not possible to fabricate CHARM®-2 sensors in GMR wafers, CHARM®-2 wafers must be substituted for, or attached to, GMR wafers. The response recorded by CHARM®-2 wafers in these situations may thus be somewhat different than the stress experienced by the GMR structures. Most likely, the difference will be in the magnitude of the response, which should allow the use of CHARM®-2 wafers for process improvement purposes through efforts which minimize the response recorded by the CHARM®-2 wafers, thereby also reducing charging levels on GMR wafers.

Establishing what levels of charging are acceptable (or excessive) in GMR process tools is more difficult. The primary reason for this is lack of detailed information about the conduction and breakdown characteristics of GMR head dielectrics. To begin with, this information is essential to select proper magnitudes of current-sensing resistors in the CHARM®-2 charge-flux sensors.

Insufficient knowledge of the breakdown modes of GMR head dielectrics also hinders proper application of CHARM®-2 data. If the GMR dielectric fails due to extremely small weak spots ("pin-holes"), the charge stored on the read head electrode may be sufficient to cause failure when a discharge potential is reached. Since the potential build-up could take place during the entire process step, the collected current density could be too small to be detected with the CHARM®-2 charge-flux sensors. Even if the stored charge is insufficient to cause failure, a pinhole current density is greatly amplified by the collection area of the read head electrode. Again, the collected current density needed to cause failure could be too small to be detected with the CHARM®-2 charge-flux sensors. In both cases, the parameter linked to read head dielectric failure would thus be the surface-substrate potential. On the other hand, if the GMR dielectric fails due to wear-out over a large area, the current density needed to cause failure will be much larger. In this case, the parameter linked to read head dielectric failure would be the collected current density, J. However, regardless of the failure mode, reducing stress levels on GMR wafers should be possible through efforts that minimize the response recorded by the CHARM®-2 wafers

V. Conclusions

Significant experience in dealing with in-process wafer charging damage (which has emerged recently in GMR head manufacturing) exists in CMOS IC manufacturing. Since the manufacturing processes and device structures in both cases are similar, a significant amount of this experience, especially as it relates to equipment characterization, should be directly applicable to the control of charging damage in GMR head manufacturing. However, we should keep in mind that, even in IC manufacturing, some charging effects are still not completely understood, and that GMR head manufacturing may add some new twists of its own.

VI. Acknowledgments

The author is indebted to Drs. A. Wallash, E. Granstrom, and R. Motta for their encouragement, suggestions, and many stimulating discussions.

VII. References

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